WHAT IS CLAIMED IS:

1. A memory wafer comprising:

a first surface having memory chips disposed thereon, the memory chips defining an exterior face of the memory wafer;

a second surface opposite the exterior face; and

a magnetically permeable shield layer extending over at least one of the exterior face and the second surface of the memory wafer.

2. The memory wafer of claim 1, wherein the memory chips are separable from the memory wafer.

3. The memory wafer of claim 1, wherein the memory chips are magnetic random access memory chips.

4. The memory wafer of claim 1, wherein the memory chips include multiple memory arrays having multiple memory cells.

5. The memory wafer of claim 4, wherein the memory cells are magnetic random access memory cells.

6. The memory wafer of claim 1, further comprising bond pads disposed on the memory chips.

7. The memory wafer of claim 6, wherein the bond pads are electrically accessible via the exterior face of the memory wafer.

8. The memory wafer of claim 1, wherein the magnetically permeable shield layer comprises a soft magnetic material.

9. The memory wafer of claim 8, wherein the soft magnetic material is selected from the group consisting of iron, nickel, cobalt, alloys of iron, alloys of nickel, and alloys of cobalt.

10. The memory wafer of claim 1, wherein the magnetically permeable shield layer has a permeability of greater than 100.

11. The memory wafer of claim 1, wherein the magnetically permeable shield layer has a coercivity of less than 10 Oersteds.

12. The memory wafer of claim 1, wherein the magnetically permeable shield layer is isotropic.

13. A memory chip separated from a memory wafer, the memory chip comprising:

at least one memory array positioned between an exterior chip face and a second chip surface opposite the exterior chip face; and

a magnetically permeable shield layer extending over at least one of the exterior chip face and the second chip surface.

14. The memory chip of claim 13, further comprising a bond pad, at least a portion of the bond pad exposed through the shield layer.

15. The memory chip of claim 13, wherein the memory chip is contained in an integrated circuit package.

16. The memory chip of claim 15, wherein the integrated circuit package includes a support for the memory chip, electrical wires connected to and leading away from the memory chip, and an insulative package encapsulating at least the memory chip.

17. The memory chip of claim 13, wherein the magnetically permeable shield layer is isotropic.

18. A method of shielding a memory device from stray magnetic fields, the method comprising:

providing a memory wafer having a plurality of separable memory chips defining an exterior face and a second surface opposite the exterior face; and

attaching a magnetically permeable shield layer over at least one of the exterior face and the second surface of the memory wafer.

19. The method of claim 18, further comprising electrically accessing bond pads disposed on the separable memory chips by a process selected from the group consisting of photolithographic patterning/etching, chemical mechanical planarization, mechanical abrasion, and chemical etching.

20. The method of claim 18, wherein attaching the magnetically permeable shield layer over at least one of the exterior face and the second surface of the memory wafer comprises a process selected from the group consisting of sputtering, evaporation, electroplating, electroless plating and chemical vapor deposition.

21. The method of claim 18, wherein attaching the magnetically permeable shield layer includes attaching the magnetically permeable shield layer in the presence of a magnetic field.

22. The method of claim 21, wherein attaching the magnetically permeable shield layer in the presence of the magnetic field includes rotating the magnetic field.

23. The method of claim 18, wherein attaching the magnetically permeable shield layer over at least one of the exterior face and the second surface of the memory wafer comprises:

depositing the magnetically permeable shield layer; and

annealing the magnetically permeable shield layer in a magnetic field.

24. The method of claim 23, wherein annealing the magnetically permeable shield layer in a magnetic field includes annealing the magnetically permeable shield layer in a rotating magnetic field.

25. The method of claim 18, wherein attaching the magnetically permeable shield layer over at least one of the exterior face and the second surface of the memory wafer comprises depositing the magnetically permeable shield layer onto a rotating memory wafer in the presence of a stationary magnetic field.

26. The method of claim 18, wherein attaching the magnetically permeable shield layer over at least one of the exterior face and the second surface of the memory wafer comprises depositing the magnetically permeable shield layer in a rotating magnetic field.

27. The method of claim 23, wherein annealing the magnetically permeable shield layer includes annealing the magnetically permeable shield layer at a temperature that is lower than an annealing temperature of a magnetic material in the memory wafer.

28. The method of claim 25, wherein depositing the magnetically permeable shield layer onto the rotating memory wafer in the presence of the stationary magnetic field forms an isotropic magnetically permeable shield layer.

29. A memory wafer comprising:

a first surface having memory chips disposed thereon, the memory chips defining an exterior face of the memory wafer;

a second surface opposite the exterior face; and

means for protecting the memory cells from stray magnetic fields.

30. The memory wafer of claim 29, wherein the means for protecting the memory cells from stray magnetic fields is a magnetically permeable shield layer comprising a soft magnetic material.

31. The memory wafer of claim 30, wherein the magnetically permeable shield layer has a permeability of greater than 100.

32. The memory wafer of claim 30, wherein the magnetically permeable shield layer has a coercivity of less than 10 Oersteds.

33. An electronic system comprising:

an electronic device; and

a memory chip electrically connected to the electronic device;

wherein the memory chip includes at least one memory array positioned between an exterior chip face and a second chip surface opposite the exterior chip face, and a magnetically permeable shield layer extending over at least one of the exterior chip face and the second chip surface.